having impurities of the same type as those in said first layer uniformly distributed therethrough; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; said first surface, said first layer and said second layer having generally coincident boundaries; [and] a plurality of diffusions of a conductivity type opposite to that of said second layer uniformly distributed into the surface of said second layer and defining p-n junctions therein and; said first layer and said second layer being epitaxial silicon layers.

10. (Twice Amended) A vertical conduction power MOSFET device having a reduced on-resistance; said device comprising a silicon substrate having a drain electrode on the bottom surface thereof, and a layer of epitaxial silicon on the upper surface of said substrate; said layer and said upper surface having generally coincident boundaries [and coextensive therewith]; said layer having a graded concentration of one of the conductivity types from its top free surface to its bottom; an upper portion of said layer extending from its free surface receiving a P-N junction which at least partly defines said power MOSFET and having an average impurity concentration which is more than the average concentration of the bottom portion of said layer; said bottom portion of said layer comprising more than 50% of the total thickness of said layer.

REMARKS

Claims 1-12 are pending in the application. No claims are allowed.

Claim Rejections Under 35 U.S.C. §112

Claims 1-12 are rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Independent claims 1 and 10 have been amended to overcome this rejection.

Claim Rejections Under 35 U.S.C. §§102 and 103

Claims 1-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muramoto. Applicants respectfully traverse this rejection. Applicants' invention, as recited in amended claim 1, is directed towards a semiconductor device comprising, inter alia,